

GA-970A-D3


Revision : 3.02

www.xinxunwei.com 400-800-9990



PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RD980 HT-LINK I/F
11	RD980 PCIE I/F ,SWITCH
12	RD980 SYSTEM I/F
13	RD980 STRAPS ,SPMEM, POWER, GND
14	RTM880T-793
15	SB950 PCIE/PCI/CPU/LPC
16	SB950 ACPI/USB/GPIO/AUDIO
17	SB950 SATA/SPI/IDE/HWM
18	SB950 POWER & GND
19	PCI EXPRESS x16
20	PCI_E x1 SLOT 1,2,3
21	PCI SLOT 1, 2
22	IT8728 EX LPC IO ,Dual-BIOS ,TPM
23	COM, F_USB, R_USB, I_PWR
24	VT2021
25	AUDIO JACK

[illegible]


			
Title COVER SHEET			
Size	Document Number	GA-970A-D3	Rev 3.02
Customer			
Date: Monday, October 08, 2012	Sheet	1	of 36

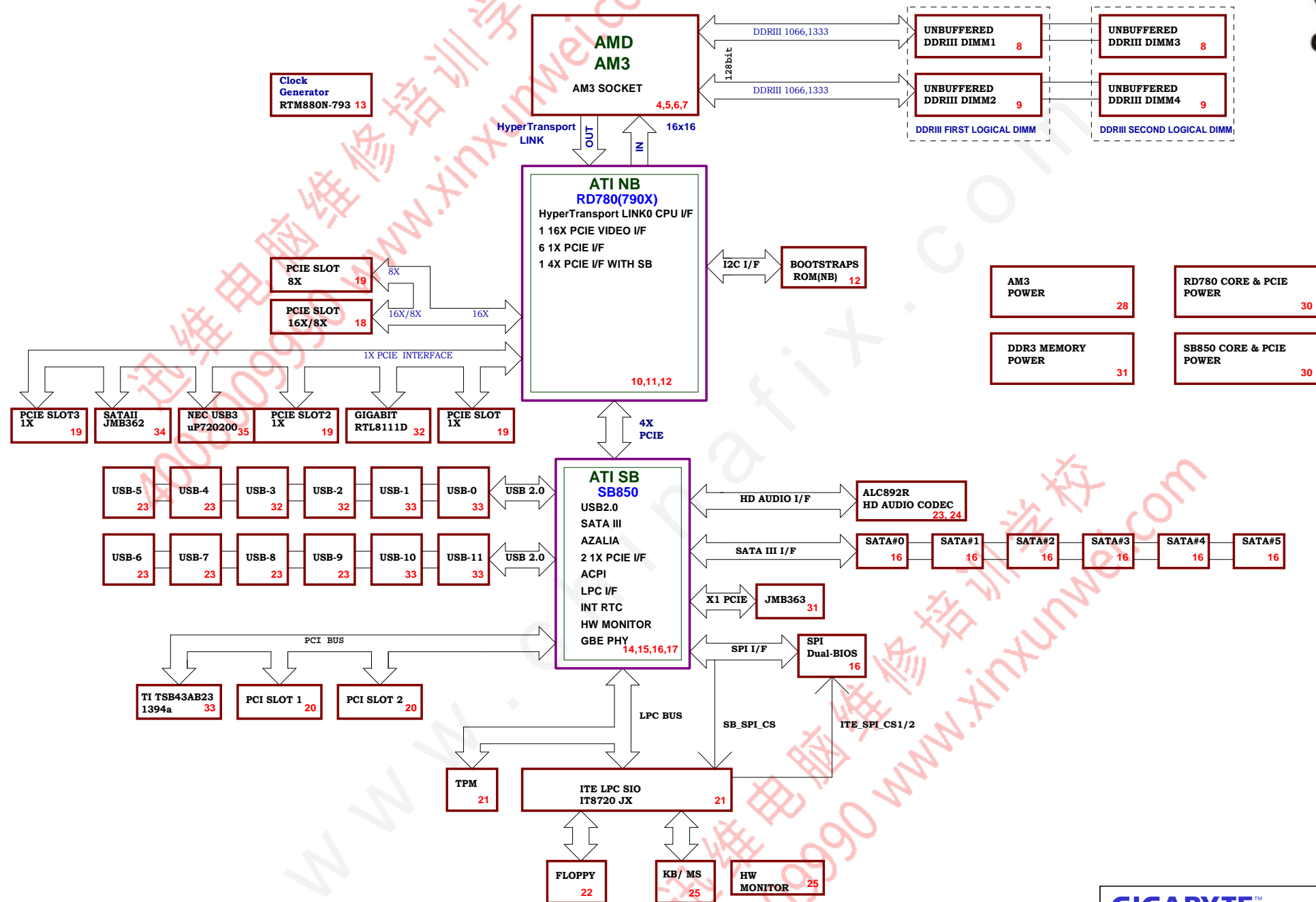
Circuit or PCB layout change for next version

P-Code: U98094-0

[illegible][illegible]

2012.10.02

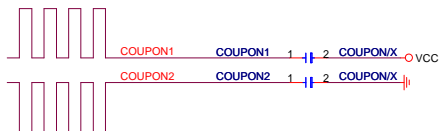
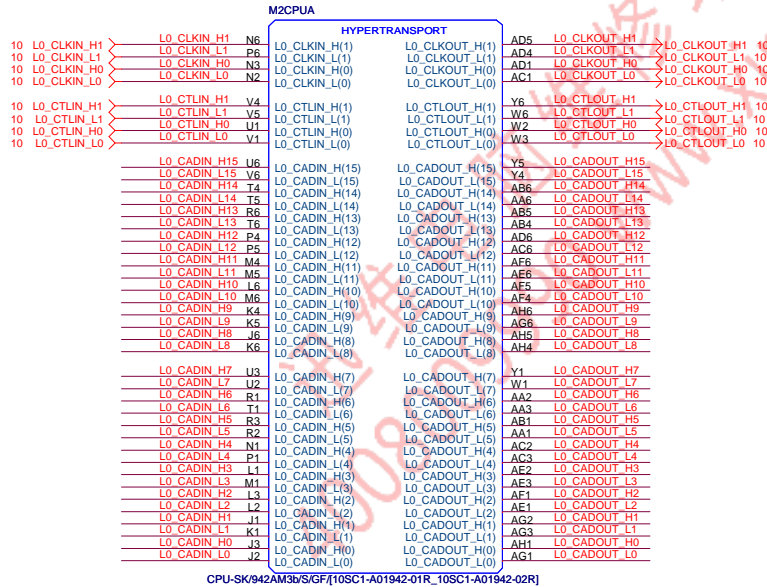
				
Title				
BOM & PCB HISTORY				
Size	Document Number			Rev
Custom	GA-970A-D3			3.02
Date:	Monday, October 08, 2012	Sheet	2 of	36



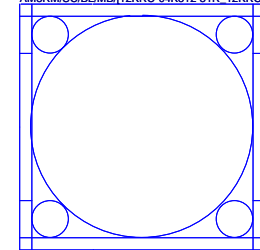
L0_CADIN_L[0..15] < L0_CADIN_L[0..15] 10
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
 VLDT_B = HT12B

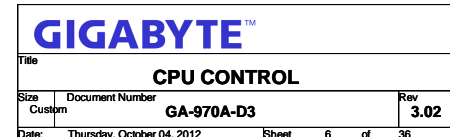


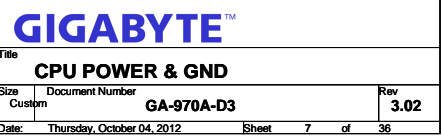
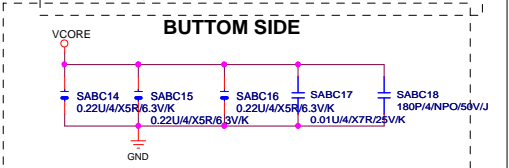
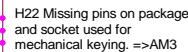
M2CPU
AM3RM/SC/BLMB/12KRC-04K812-31R_12KRC-04K812-32R



GIGABYTE™

Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-970A-D3	3.02	
Date:	Thursday, October 04, 2012	Sheet	4 of 36

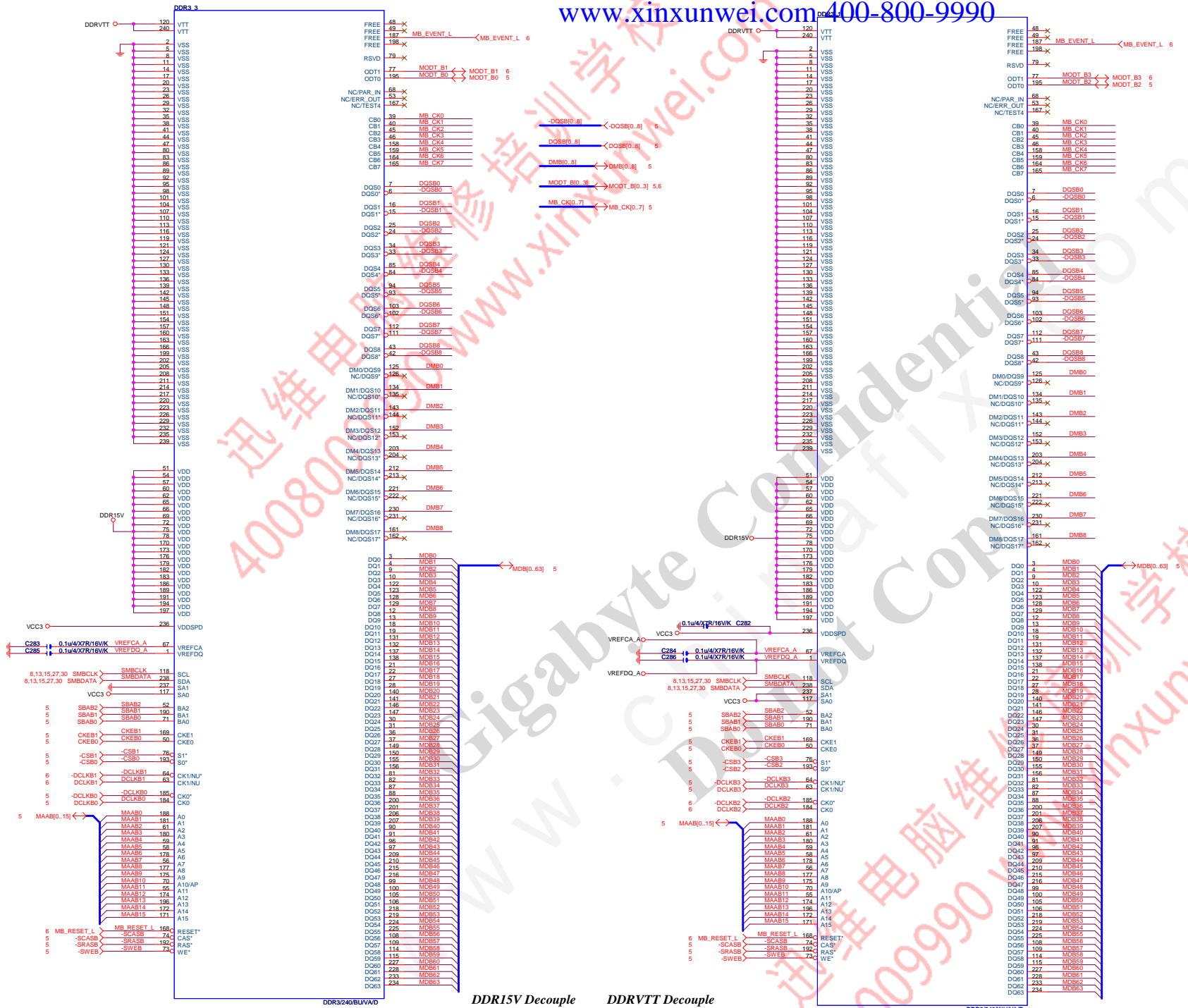




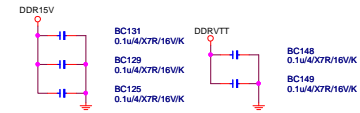




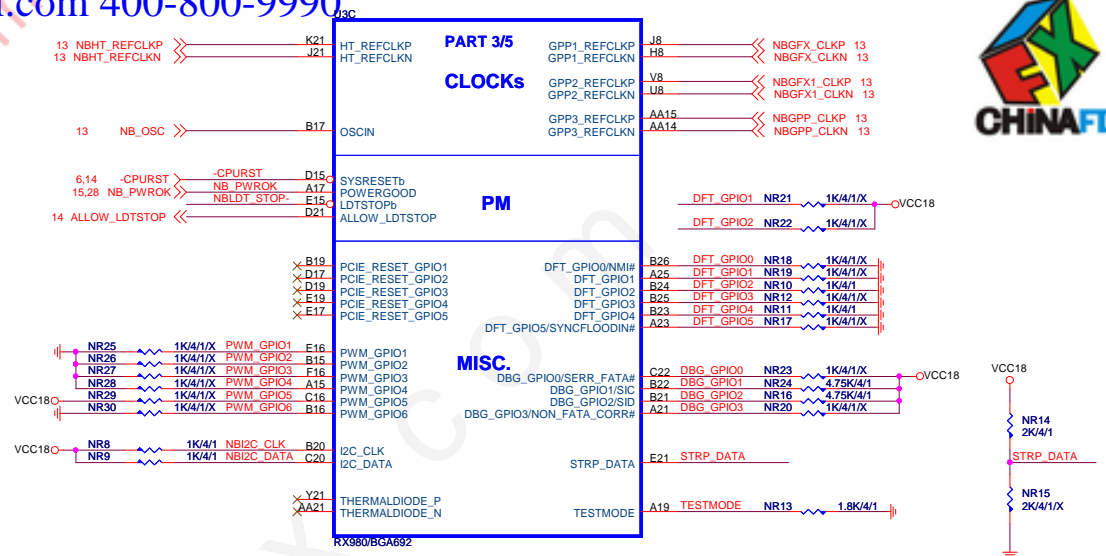
www.xinxunwei.com 400-800-9990




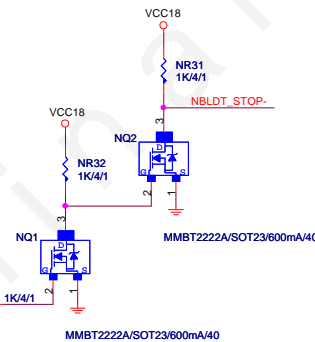
DDR15V Decouple DDRVTT Decouple



GIGABYTE	
Title: DDR III CHANNEL B	
Size: GA-970A-D3	Rev: 3.02
Doc: GA-970A-D3	
Date: Thursday, October 04, 2012	Sheet: 9 of 35



			
Title			
RS780 HT-LINK I/F			
Size	Document Number	Rev	
Custom	GA-970A-D3	3.02	
Date:	Thursday, October 04, 2012	Sheet	10 of 36



U3B

PART 2/5

EXP A_RXP15 N6
EXP A_RXN15 N5
EXP A_RXP14 M5
EXP A_RXN14 M4
EXP A_RXP13 L6
EXP A_RXN13 L5
EXP A_RXP12 K5
EXP A_RXN12 K4
EXP A_RXP11 J6
EXP A_RXN11 J5
EXP A_RXP10 H5
EXP A_RXN10 H4
EXP A_RXP9 G6
EXP A_RXN9 G5
EXP A_RXP8 F5
EXP A_RXN8 F4
EXP A_RXP7 D2
EXP A_RXN7 D1
EXP A_RXP6 B5
EXP A_RXN6 B4
EXP A_RXP5 C6
EXP A_RXN5 E6
EXP A_RXP4 E7
EXP A_RXN4 F7
EXP A_RXP3 D8
EXP A_RXN3 E8
EXP A_RXP2 E9
EXP A_RXN2 F9
EXP A_RXP1 D10
EXP A_RXN1 E10
EXP A_RXP0 E11
EXP A_RXN0 F11

PCIE GPP1

GPP1_RX15P
GPP1_RX15N
GPP1_RX14P
GPP1_RX14N
GPP1_RX13P
GPP1_RX13N
GPP1_RX12P
GPP1_RX12N
GPP1_RX11P
GPP1_RX11N
GPP1_RX10P
GPP1_RX10N
GPP1_RX9P
GPP1_RX9N
GPP1_RX8P
GPP1_RX8N
GPP1_RX7P
GPP1_RX7N
GPP1_RX6P
GPP1_RX6N
GPP1_RX5P
GPP1_RX5N
GPP1_RX4P
GPP1_RX4N
GPP1_RX3P
GPP1_RX3N
GPP1_RX2P
GPP1_RX2N
GPP1_RX1P
GPP1_RX1N
GPP1_RX0P
GPP1_RX0N

N3 EXP A_TXP15
M2 EXP A_TXP14
M1 EXP A_TXN14
L3 EXP A_TXP13
L2 EXP A_TXN13
K2 EXP A_TXP12
K1 EXP A_TXN12
J3 EXP A_TXP11
J2 EXP A_TXN11
H2 EXP A_TXP10
H1 EXP A_TXN10
G3 EXP A_TXP9
G2 EXP A_TXN9
F2 EXP A_TXP8
F1 EXP A_TXN8
E3 EXP A_TXP7
E2 EXP A_TXN7
A4 EXP A_TXP6
B4 EXP A_TXN6
A6 EXP A_TXP5
B6 EXP A_TXN5
B7 EXP A_TXP4
C7 EXP A_TXN4
A8 EXP A_TXP3
B8 EXP A_TXN3
B9 EXP A_TXP2
C9 EXP A_TXN2
A10 EXP A_TXP1
B10 EXP A_TXN1
B11 EXP A_TXP0
C11 EXP A_TXN0

AC9
AD9
AE8
AC7
AD7
AD6
AE6
AE5
AG5
AF2
AF1
AD2
AD1
AB5
AB4
AA6
AA5
Y5
Y4
W6
W5
V5
V4
U6
U5
T5
T4
R6
R5
P5
P4

PCIE GPP2

GPP2_RX15P
GPP2_RX15N
GPP2_RX14P
GPP2_RX14N
GPP2_RX13P
GPP2_RX13N
GPP2_RX12P
GPP2_RX12N
GPP2_RX11P
GPP2_RX11N
GPP2_RX10P
GPP2_RX10N
GPP2_RX9P
GPP2_RX9N
GPP2_RX8P
GPP2_RX8N
GPP2_RX7P
GPP2_RX7N
GPP2_RX6P
GPP2_RX6N
GPP2_RX5P
GPP2_RX5N
GPP2_RX4P
GPP2_RX4N
GPP2_RX3P
GPP2_RX3N
GPP2_RX2P
GPP2_RX2N
GPP2_RX1P
GPP2_RX1N
GPP2_RX0P
GPP2_RX0N

AF9
AG9
AG8
AH8
AF7
AG7
AG6
AH6
AG4
AH4
AE3
AE2
AC3
AC2
AB2
AB1
AA3
AA2
Y2
Y1
W3
W2
V2
V1
U3
U2
T2
T1
R3
R2
P2
P1

AD11
AC11
AE12
AD13
AC13
AE14
AD14
AD15
AC15
AE16
AD16
AD17
AC17
AE18
AD18
AD19
AC19
AH20
AG20

PCIE GPP3

GPP3_RX9P
GPP3_RX9N
GPP3_RX8P
GPP3_RX8N
GPP3_RX7P
GPP3_RX7N
GPP3_RX6P
GPP3_RX6N
GPP3_RX5P
GPP3_RX5N
GPP3_RX4P
GPP3_RX4N
GPP3_RX3P
GPP3_RX3N
GPP3_RX2P
GPP3_RX2N
GPP3_RX1P
GPP3_RX1N
GPP3_RX0P
GPP3_RX0N

AH10
AG10
AG11
AE15
AH12
AG12
AG13
AE13
AH14
AG14
AG15
AG16
AH15
AG16
AG17
AG17
AG18
AG18
AG19
AG19
AF19

PCI E slot TX need CAP close to slot side

EXP A_TXP[0..15] >> EXP_A_TXP[0..15] 18
EXP A_TXN[0..15] >> EXP_A_TXN[0..15] 18
EXP A_RXP[0..15] >> EXP_A_RXP[0..15] 18
EXP A_RXN[0..15] >> EXP_A_RXN[0..15] 18

19 PCIE5_IP
19 PCIE5_IN
33 ML_IP
33 ML_IN
19 PCIE2_IP
19 PCIE2_IN
19 PCIE1_IP
19 PCIE1_IN
31 USB3_IP
31 USB3_IN

PCIE ALINK

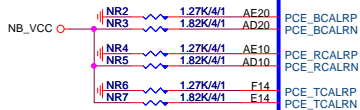
SB_RX3P
SB_RX3N
SB_RX2P
SB_RX2N
SB_RX1P
SB_RX1N
SB_RX0P
SB_RX0N

AG22
AH22
AE21
AG21
AF23
AG23
AG24
AH24

A_TX3P C NC11
A_TX3N C NC12
A_TX2P C NC14
A_TX2N C NC13
A_TX1P C NC15
A_TX1N C NC16
A_TX0P C NC18
A_TX0N C NC17

A_TX3P 14
A_TX3N 14
A_TX2P 14
A_TX2N 14
A_TX1P 14
A_TX1N 14
A_TX0P 14
A_TX0N 14

PLACE THESE CAP CLOSE TO NB.

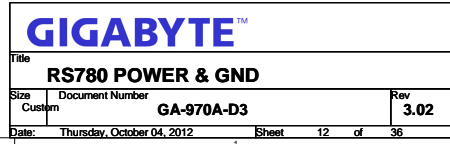


RX980/BGA692

GIGABYTE™

Title
RS780 PCIE I/F ,SwitchSize Document Number
Custom GA-970A-D3Rev
3.02

Date: Thursday, October 04, 2012 Sheet 11 of 36



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* the GFX_REFCLK input is required for all cases

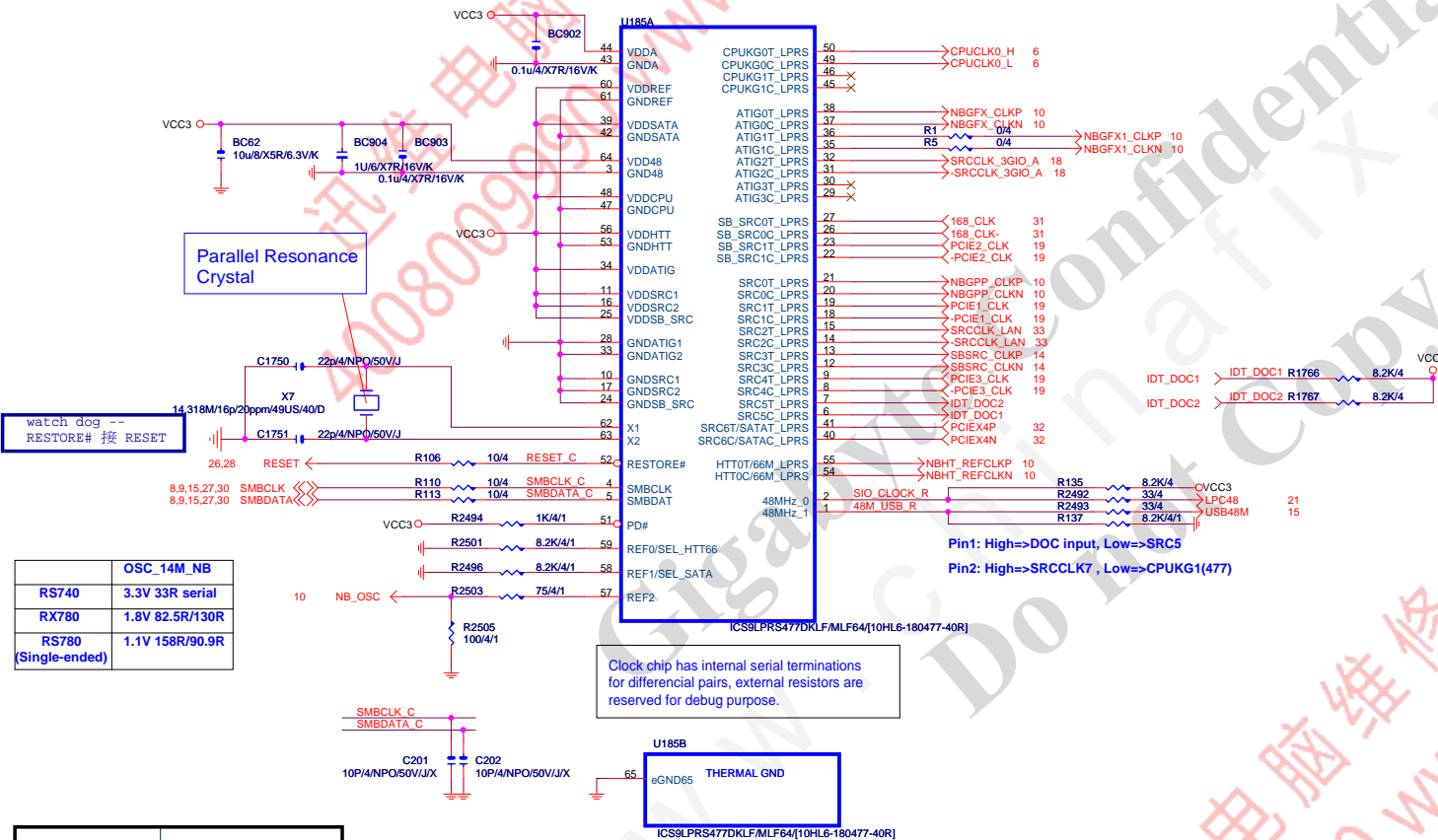


1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE TO U800 AS
POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx
AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800
POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair




GIGABYTE™

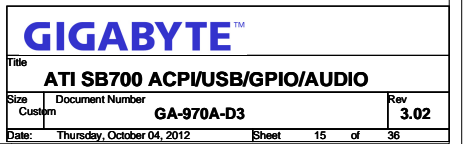
Title
RTM880N-793Size
Custom
Document Number
GA-970A-D3Rev
3.02

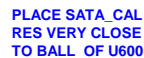
Date: Thursday, October 04, 2012 Sheet 13 of 36

low PCIE GEN2

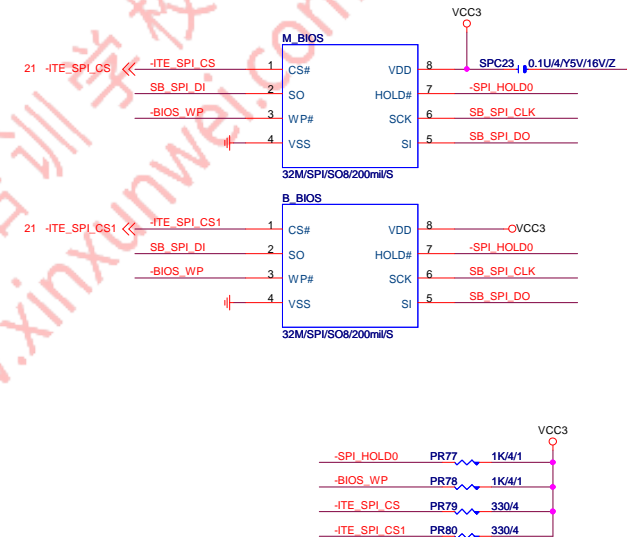
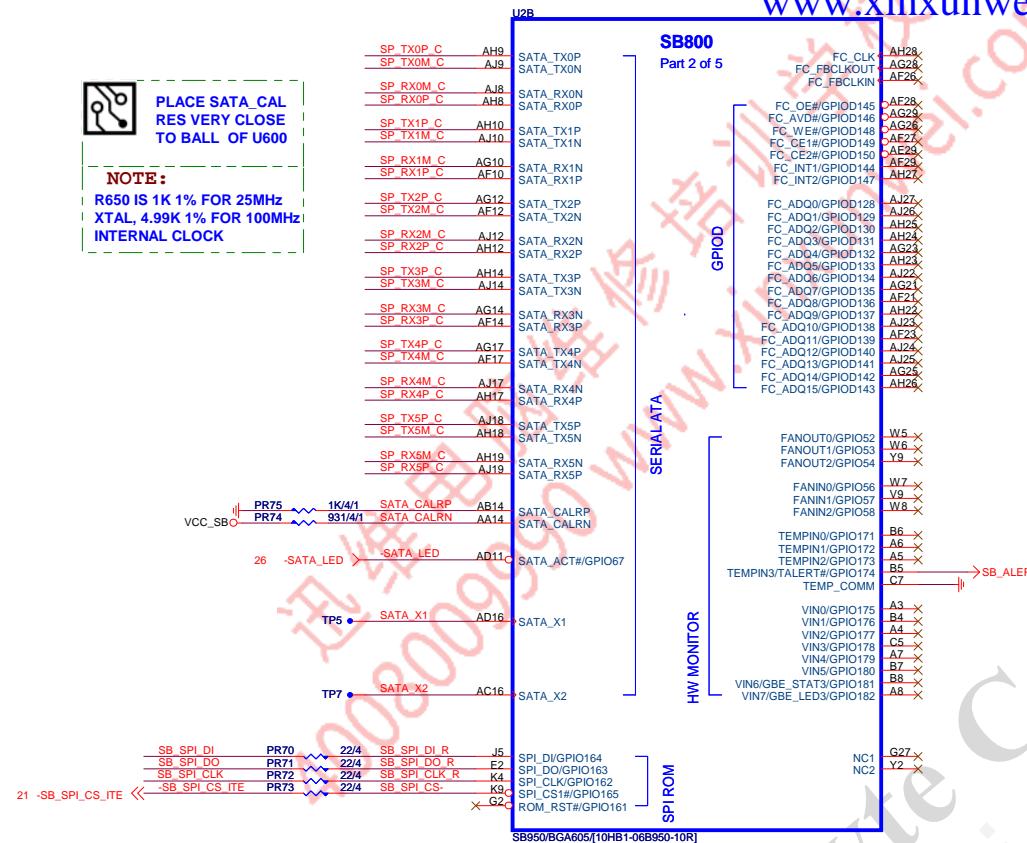


			
Title			
ATI SB700 PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-970A-D3	3.02	
Date:	Thursday, October 04, 2012	Sheet	14 of 36





NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

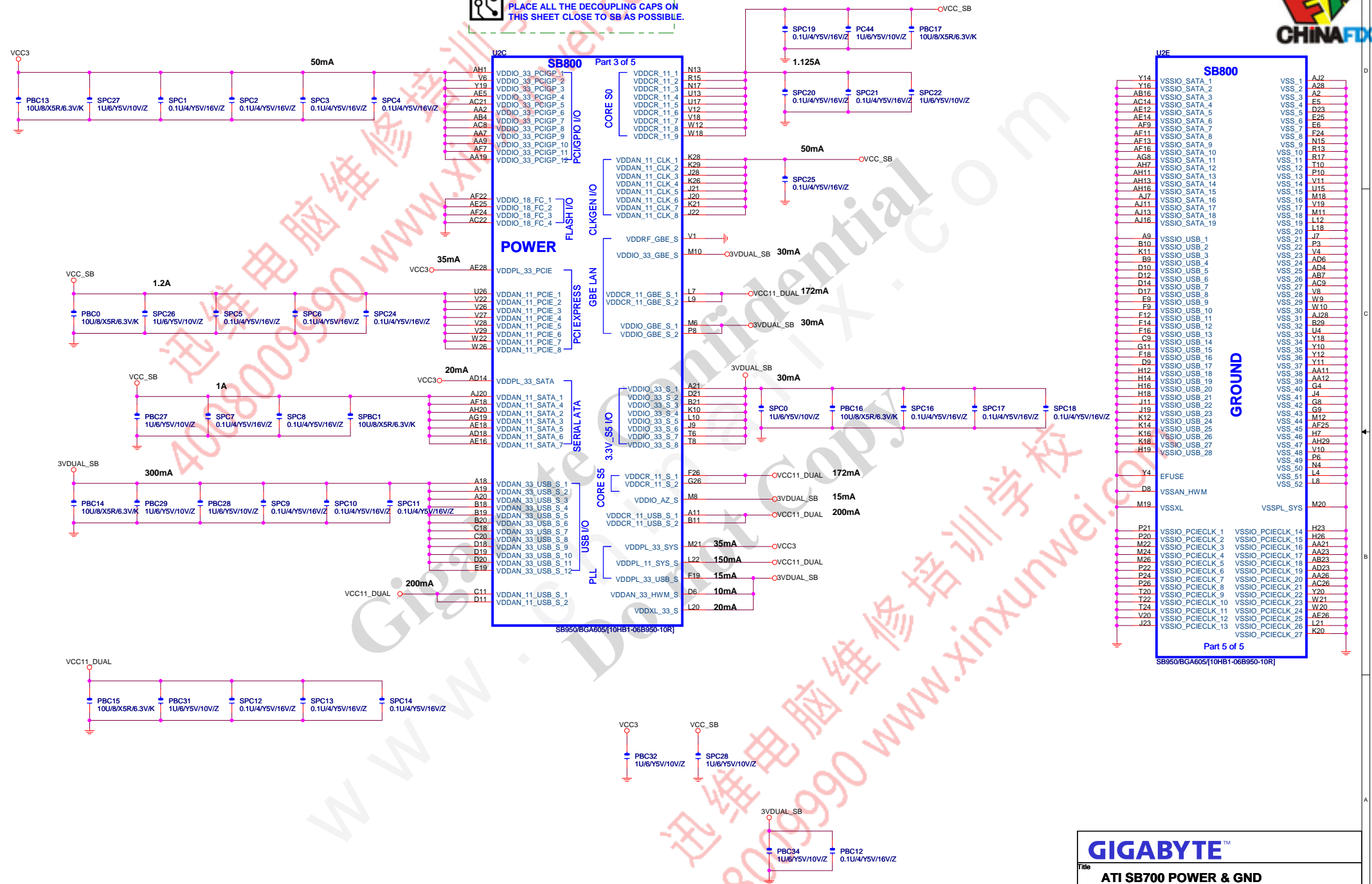


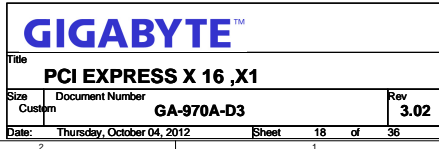
Title	ATI SB700 SATA/IDE/HWM/SPI
-------	----------------------------

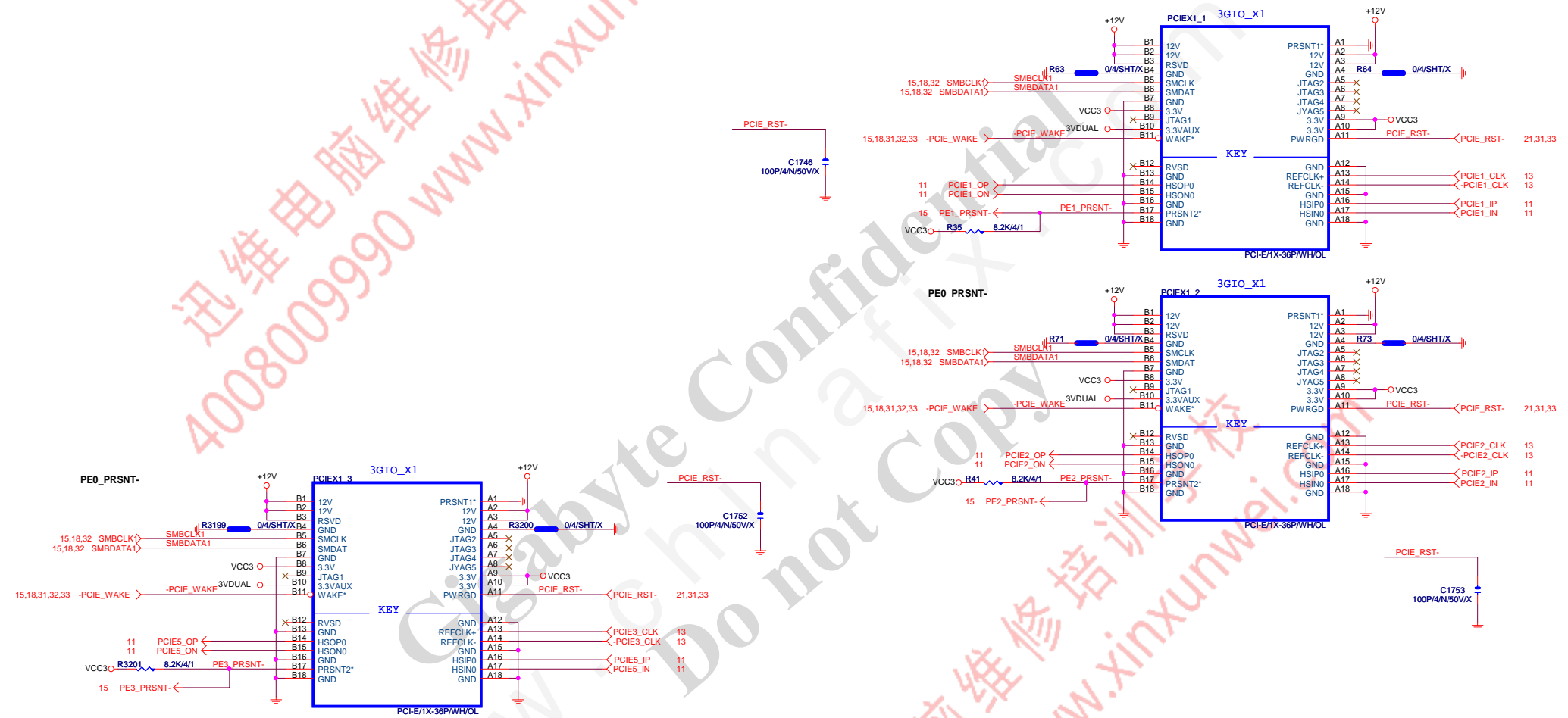
Size Custom	Document Number GA-970A-D3	Rev 3.02
Date:	Thursday, October 04, 2012	Sheet 16 of 36



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.






GIGABYTE™

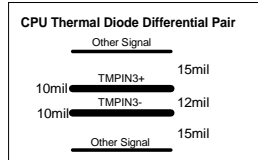
PCI_E x8 ,PCI_E x1 SLOT 1,2

Size	Document Number	Rev
Custom	GA-970A-D3	3.02
Date:	Thursday, October 04, 2012	Sheet 19 of 36

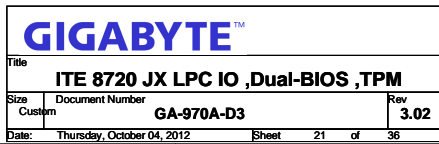
PCI SLOT2

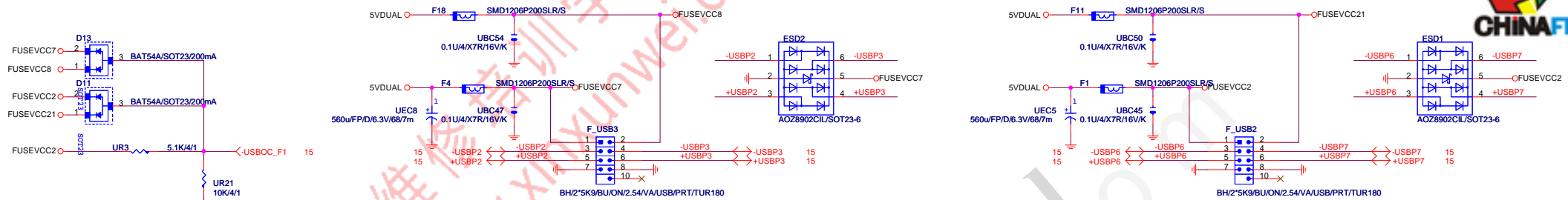


Date: Thursday, October 04, 2012 Sheet 20 of 36



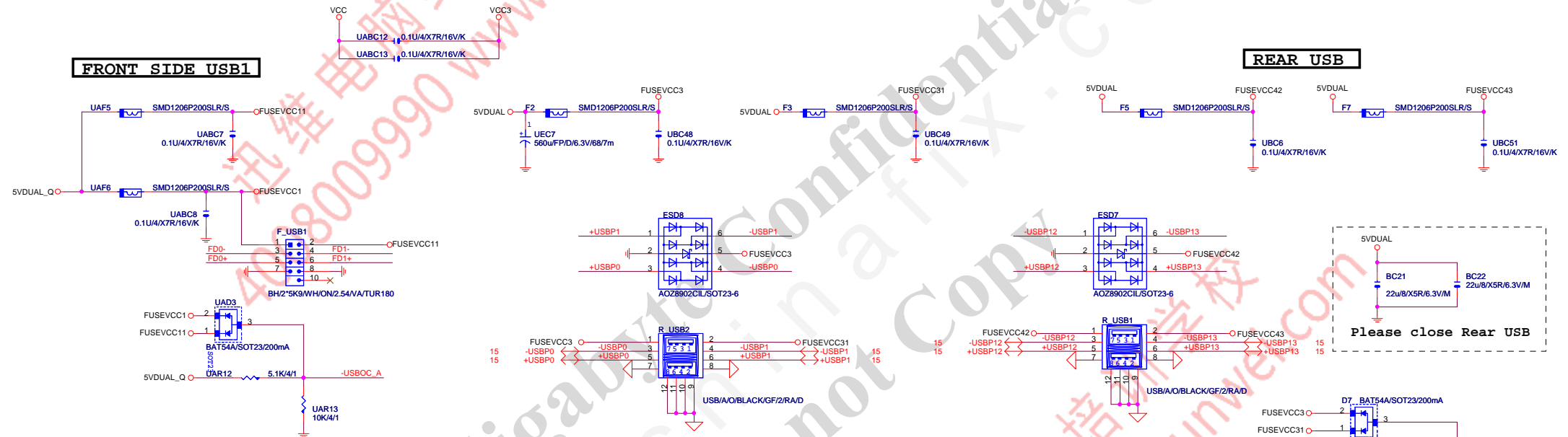
	Symbol	value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin 79		0	DSW
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin 25		0	Enable WDT to rest PWROK
JP3	FAN_CTL_SEL	1	The default value of EC Index 63h/6Bh/73h is 80h
Pin 27		0	The default value of EC Index 15h/16h/17h is 40h
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 29		0	K8 power sequence function is enabled
JP5	UOVMODE_SEL	1	NOTICE TYPE
Pin 60		0	FORCE TYPE
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
Pin 101		0	Disable Dual BIOS Function for GigaByte Only





FRONT SIDE USB1

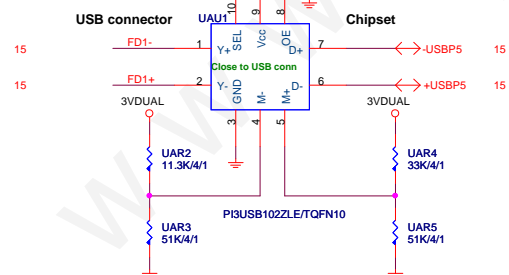
REAR USB



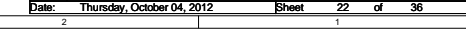
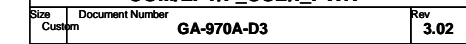
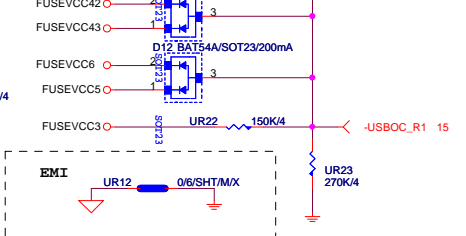
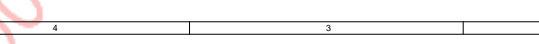
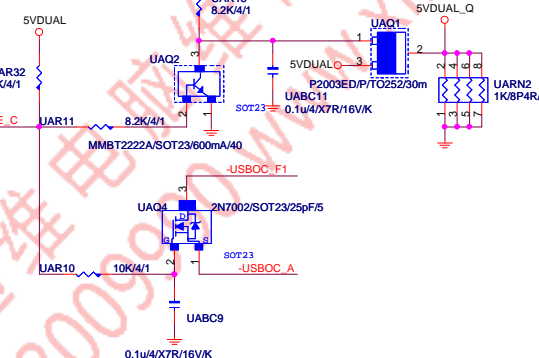
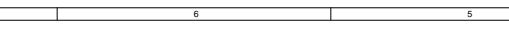
Please close Rear USB

I_Phone charger circuit

DEFAULT H, STABBY POWER

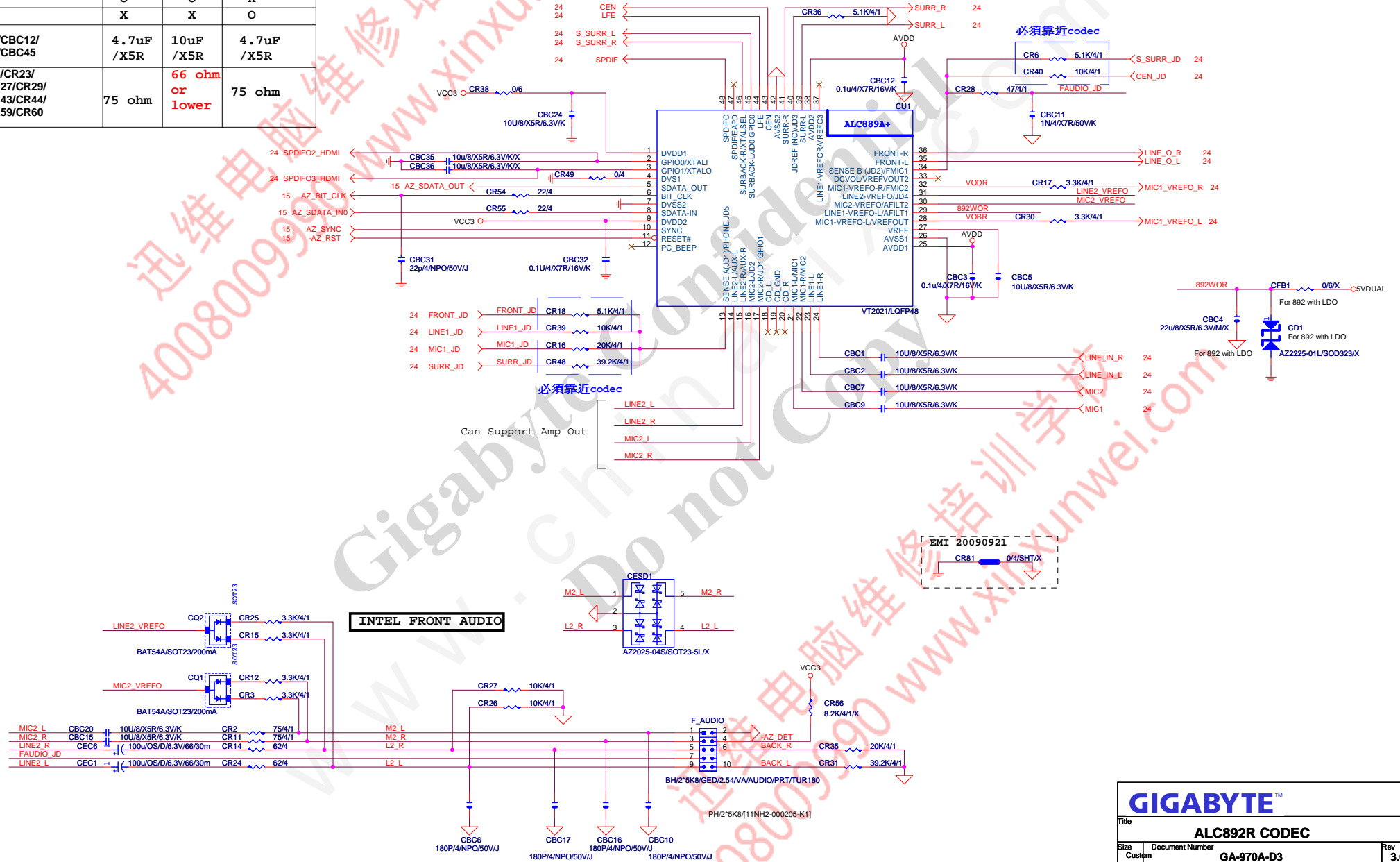


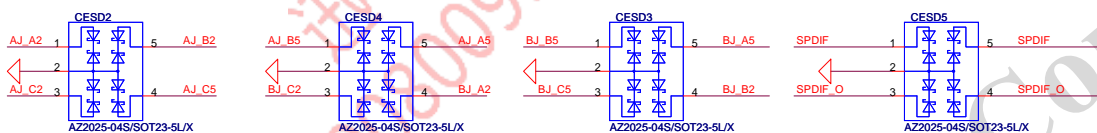
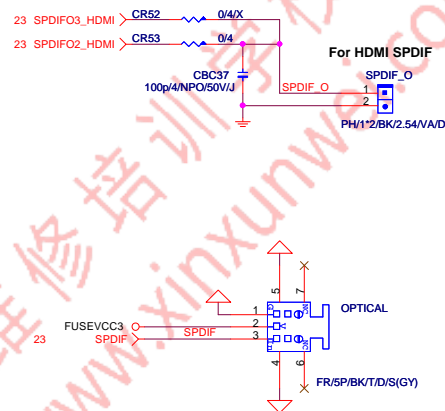
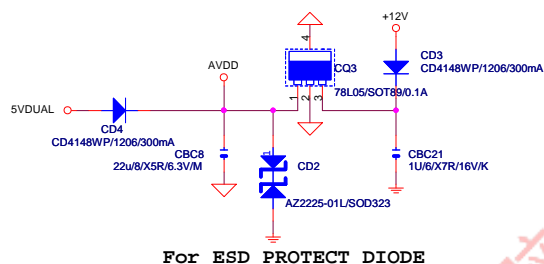
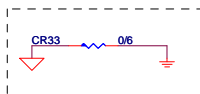
DEFAULT H, STABBY POWER



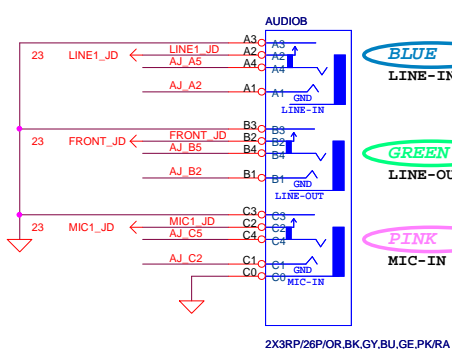
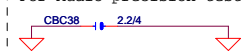


	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

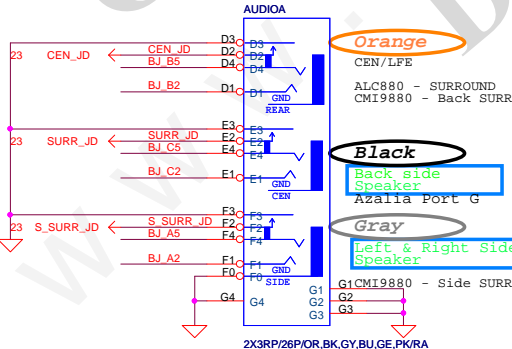
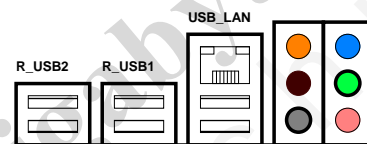




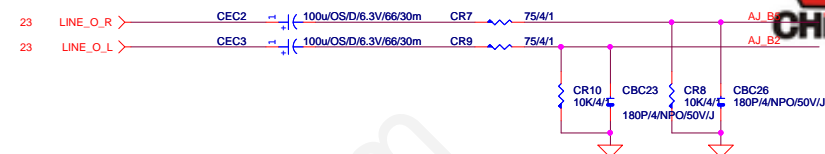
For Audio precision test



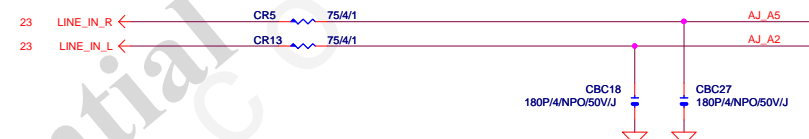
A3R7/13P/B/[[11NR6-403006-01_11NR6-403006-02]
3R3+15P/[[11NR6-403004-11]]



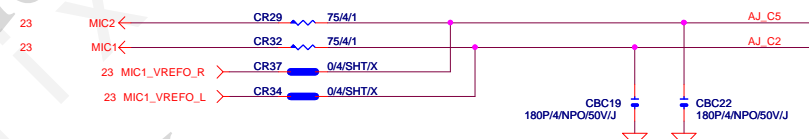
A3R7/13P/0BG/[[11NR6-403006-71]
3R3+15P/[[11NR6-403004-31]]

LINE OUT
FRONT OUT

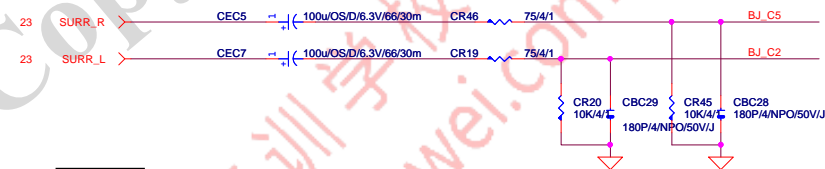
LINE-IN



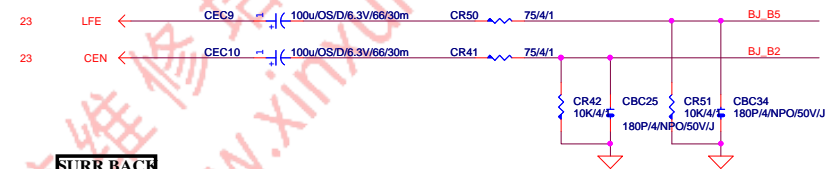
MIC



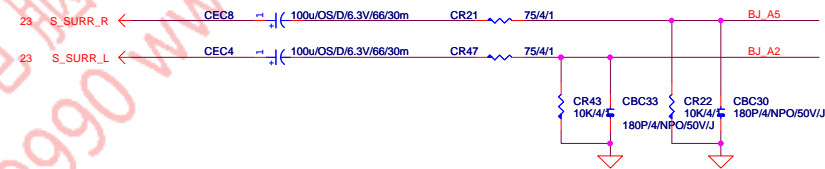
SURROUND



CEN/LFE



SURR BACK

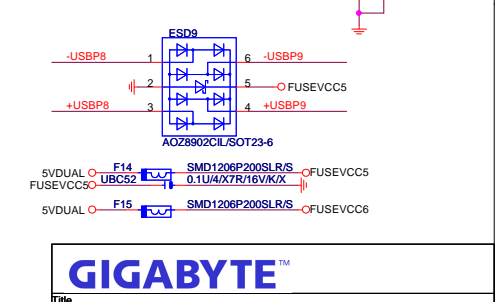
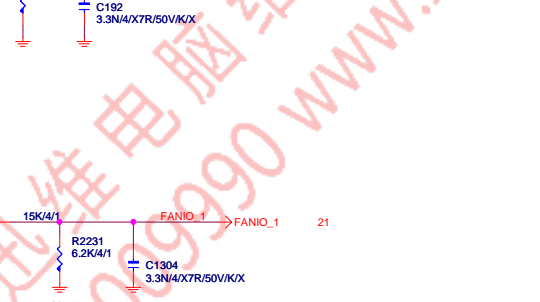
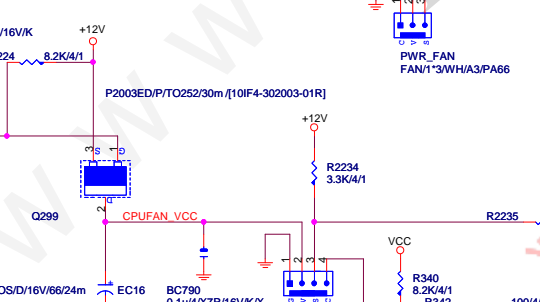
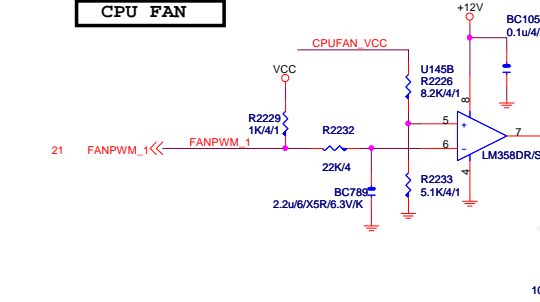
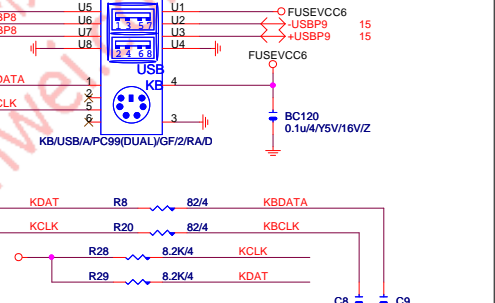
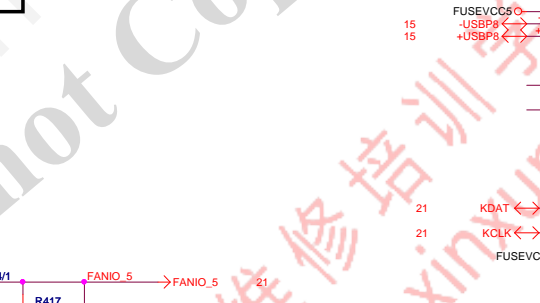
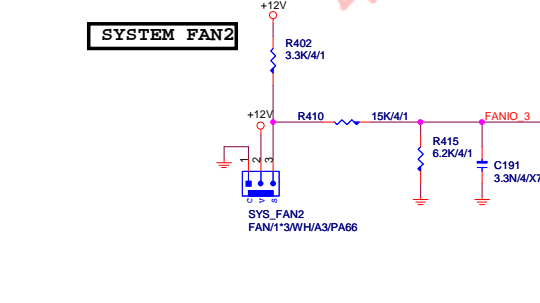
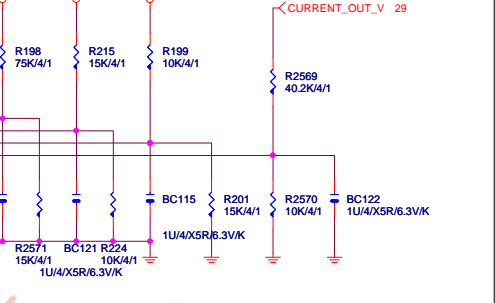
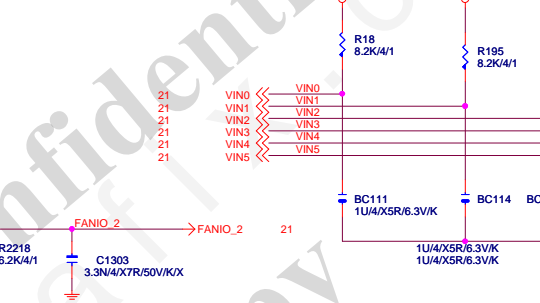
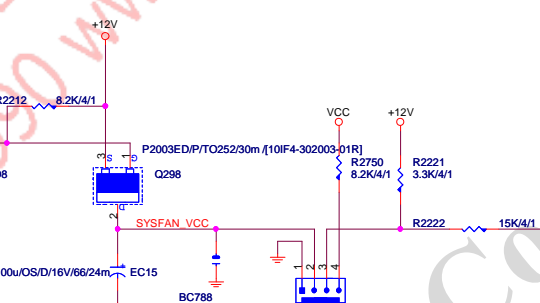
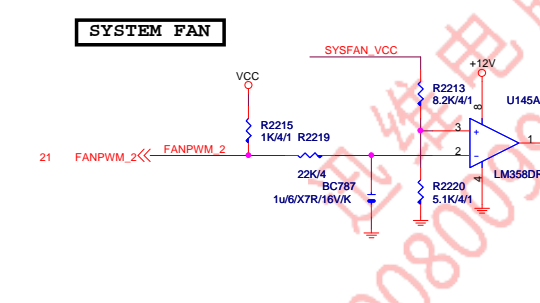
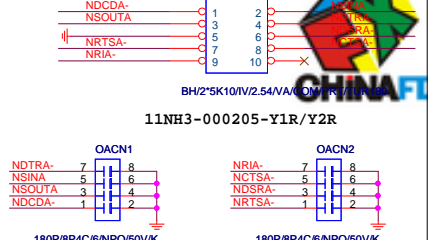
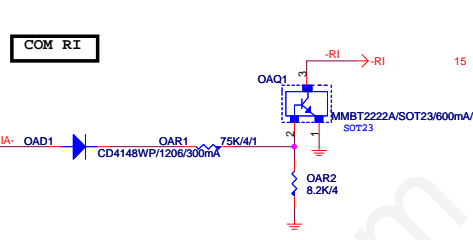
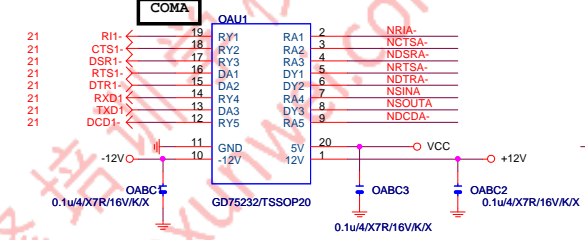
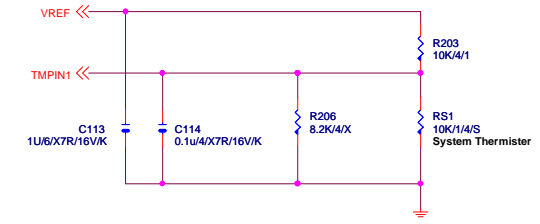


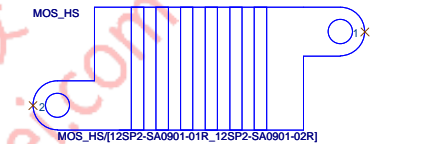
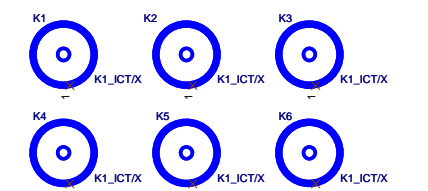
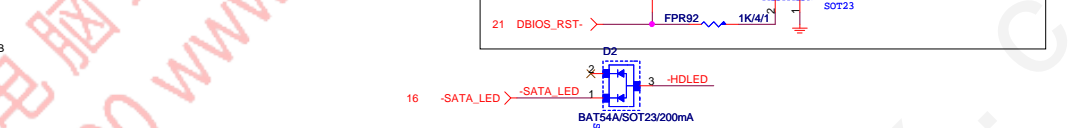
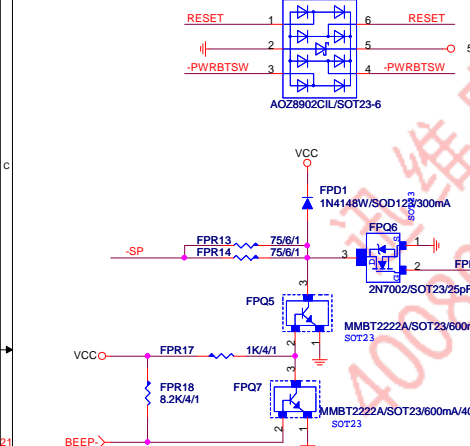
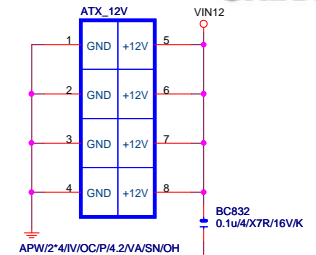
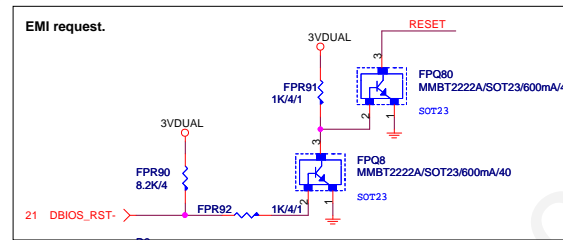
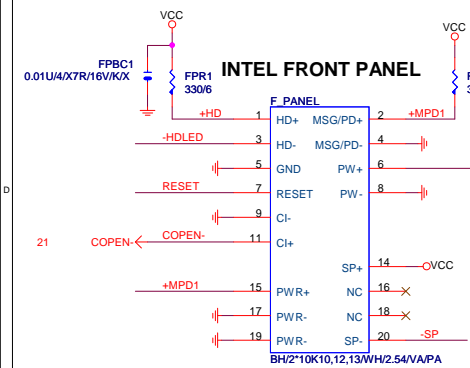
GIGABYTE™

Title
AUDIO JACKSize
Customer Document Number
GA-970A-D3Rev
3.02

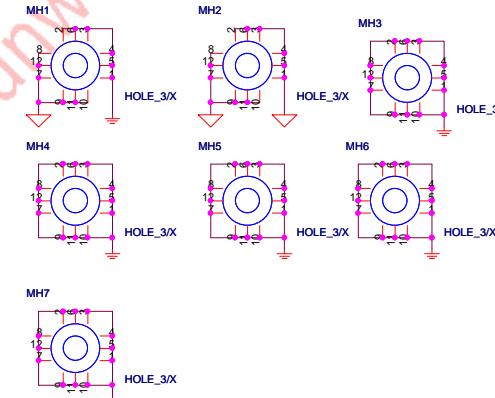
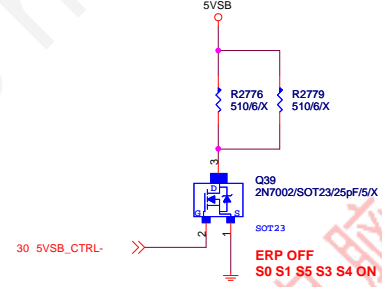
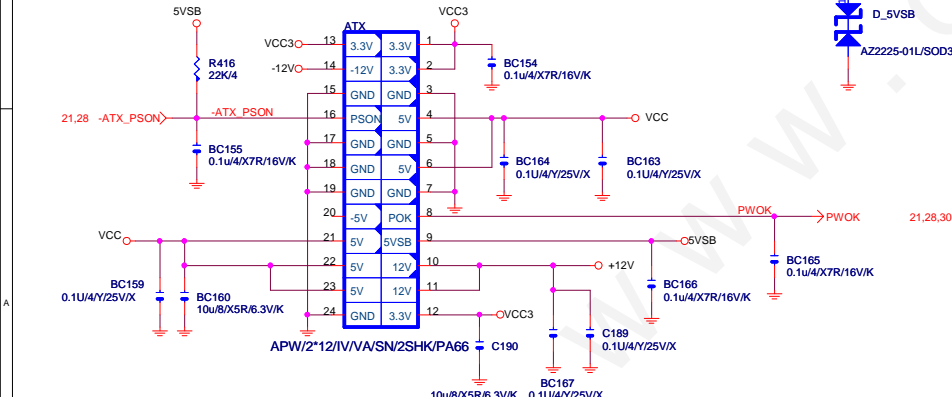
Date: Thursday, October 04, 2012 Sheet 24 of 36

Hardware Monitor circuits

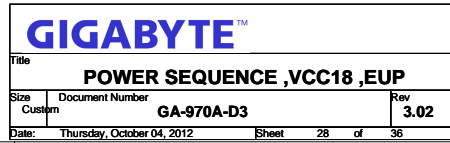


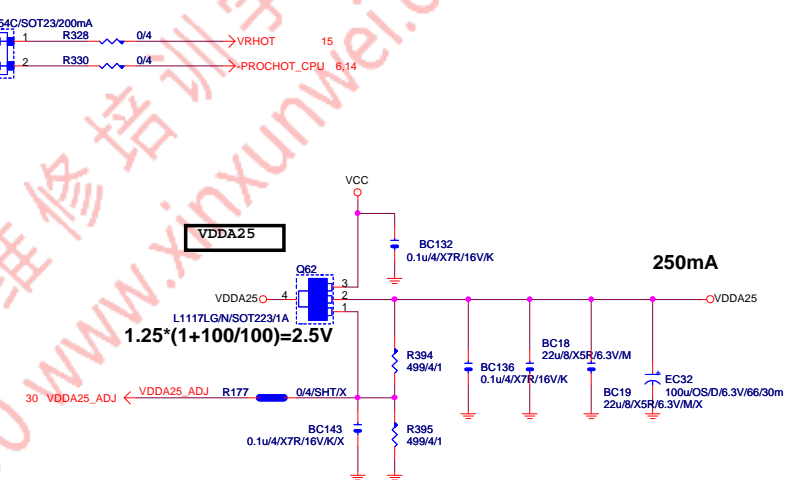
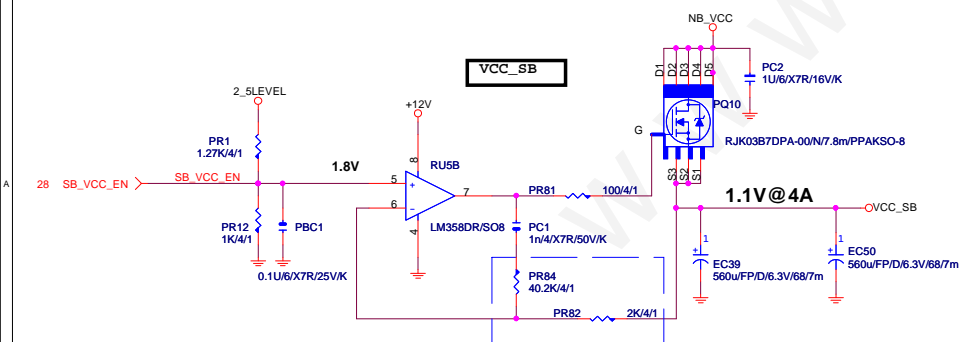
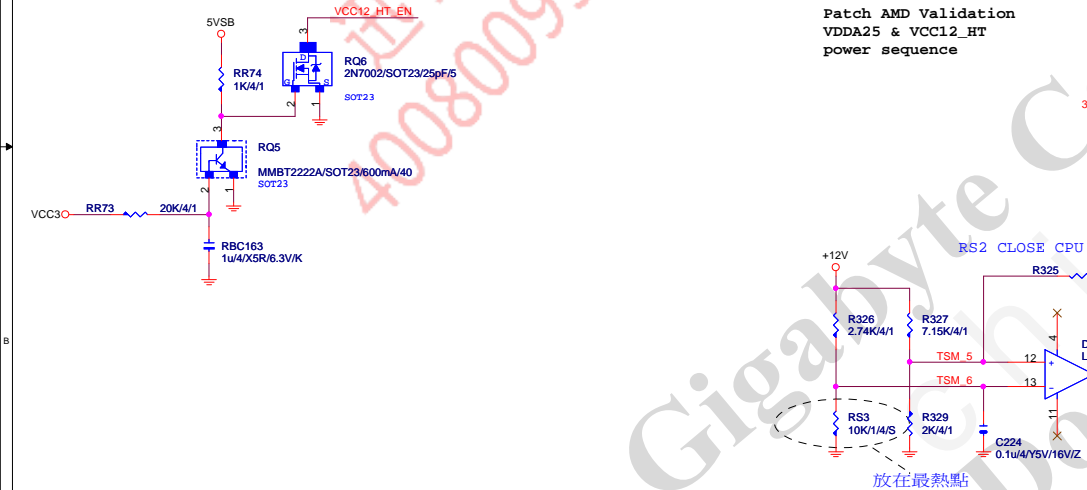
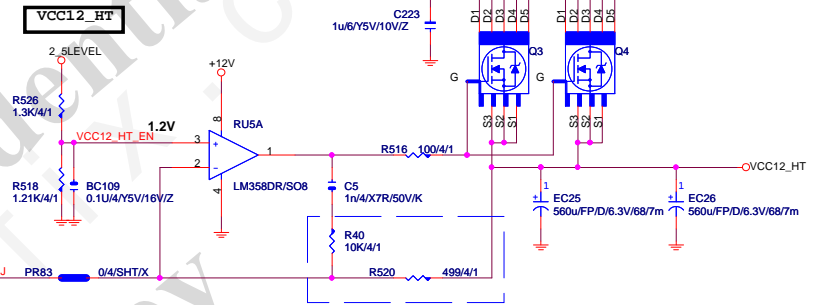
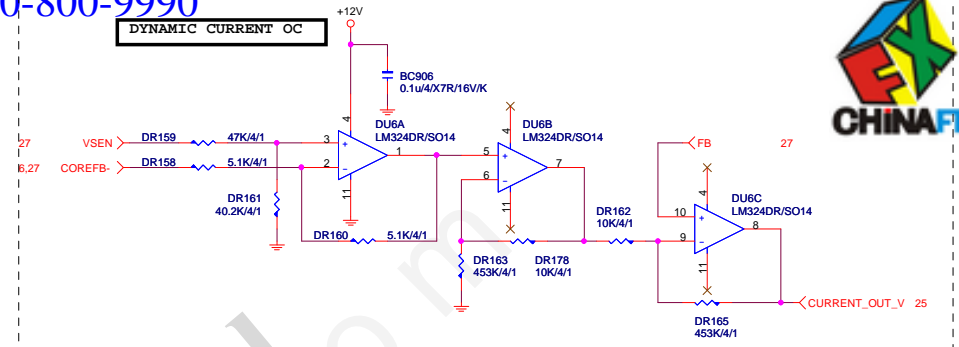
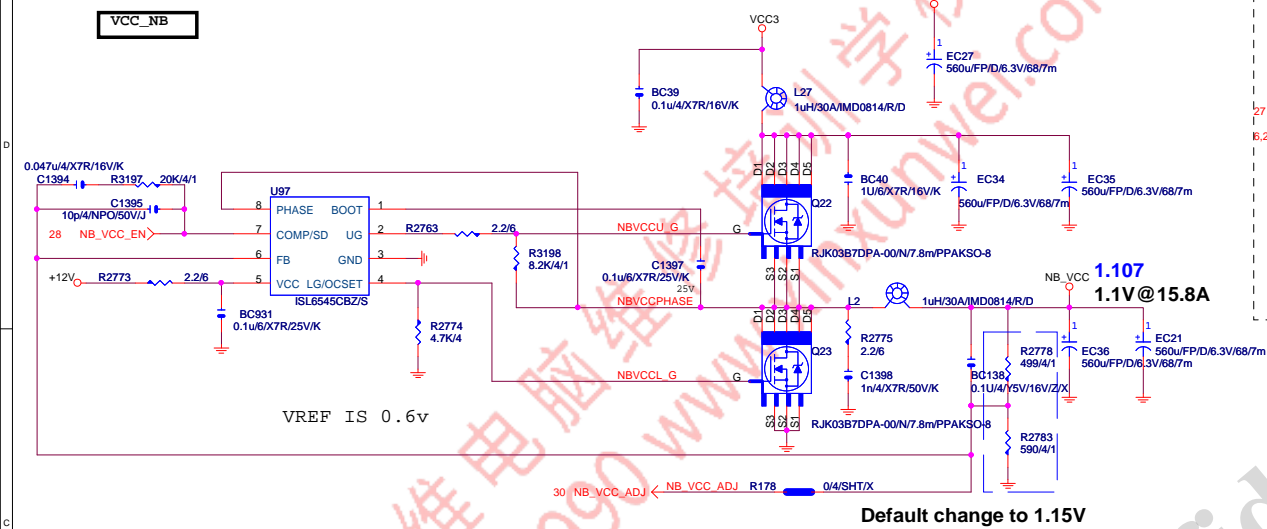


ATX POWER CONNECTOR



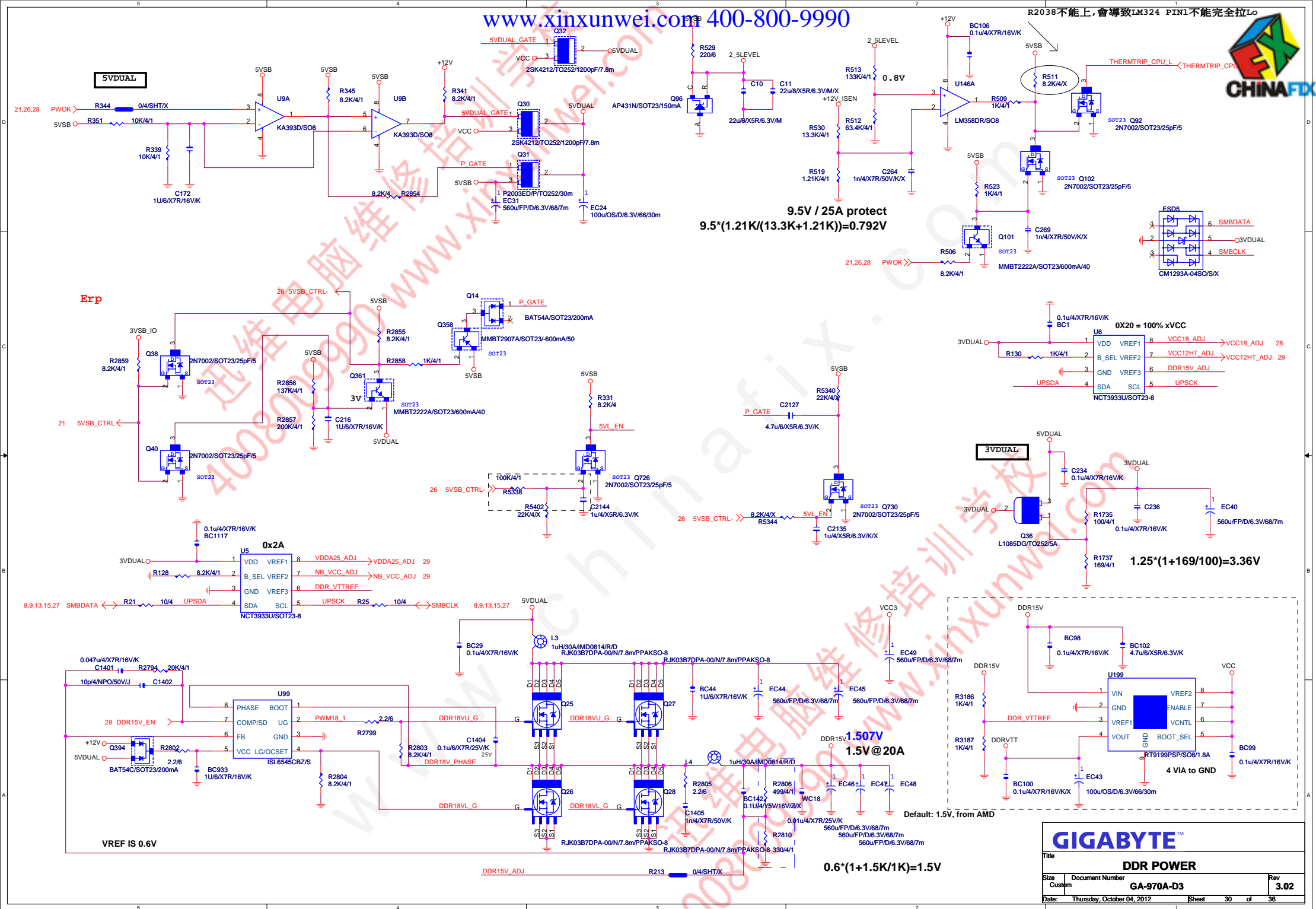






GIGABYTE

Title			
NB/SB POWER,VCC12HT,VDDA25,VCC12Dual			
Size	Document Number	Rev	
Custom	GA-970A-D3	3.02	
Date:	Thursday, October 04, 2012	Sheet	29 of 36



GIGABYTE

Title			DDR POWER
Size	Document Number	Rev	
Custom	GA-970A-D3	3.02	
Date:	Thursday, October 04, 2012	Sheet	30 of 36

